IN THE CLAIMS:

Claims 16 through 26 were previously cancelled. Claim 7 has been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Previously presented) A method for generating a wafer level burn-in reliability curve, comprising:

detecting a signal indicating a transition associated with one of a number *m* of cycles of burn-in testing of a wafer;

storing a time stamp associated with the transition in nonvolatile memory in each integrated circuit (IC) die on the wafer;

performing a built-in self test (BIST) to determine a current number of failures in the each IC die associated with the time stamp;

storing the current number of failures in the each IC die associated with the time stamp in the nonvolatile memory in the each IC die;

repeating the foregoing for at least one additional cycle of burn-in testing; and

reading each time stamp and the current number of failures associated with the time stamp for each at least one additional cycle.

2. (Previously presented) The method according to claim 1, wherein the signal indicating the transition associated with one of the number *m* of cycles of burn-in testing comprises a supervoltage signal.

3. (Previously presented) The method according to claim 1, wherein the number *m* of cycles comprises four quarters of burn-in testing.

4. (Previously presented) The method according to claim 1, wherein the transition occurs before a first time stamp, between two consecutive time stamps, or after a last time stamp of the number *m* of cycles of burn-in testing.

5. (Previously presented) The method according to claim 1, wherein the wafer comprises a plurality of integrated circuits.

6. (Previously presented) The method according to claim 5, wherein each of the plurality of integrated circuits comprises a memory device.

7. (Currently amended) The method according to claim 1, wherein reading ~~the~~ each time stamp and the current number of failures associated with the time stamp for each IC die on the ~~waver~~ wafer comprises reading nonvolatile elements at wafer probe testing.

8. (Previously presented) The method according to claim 1, further comprising generating the wafer level burn-in reliability curve from the time stamp and the each time stamp and the current number of failures associated with the one of a number of *m* cycles and the at least one additional cycle of burn-in testing.

9. (Previously presented) A method for testing a wafer having integrated circuit (IC) dice formed thereon, comprising:

stressing the IC dice;

storing wafer level burn-in reliability data in nonvolatile elements in each IC die on the wafer; and

performing a wafer probe procedure comprising:

executing a functional test to identify error-free IC dice and repairable IC dice from the IC dice;

repairing all repairable IC dice; and

reading wafer level burn-in reliability data stored in the nonvolatile elements.

10. (Previously presented) The method according to claim 9, wherein stressing, storing and performing are performed in the order stated.

11. (Previously presented) The method according to claim 9, wherein stressing comprises using built-in self-stress circuitry in each IC die.

12. (Previously presented) The method according to claim 9, further comprising generating burn-in reliability curves from the wafer level burn-in reliability data.

13. (Previously presented) The method according to claim 12, further comprising determining whether to scrap the wafer, to scrap a lot including the wafer or to identify a need for additional burn-in.

14. (Previously presented) The method according to claim 9, wherein stressing the IC dice comprises elevating a power supply voltage with respect to a nominal operating voltage.

15. (Previously presented) The method according to claim 9, further comprising:

forming a sacrificial metal layer for delivering power to the IC dice on the wafer prior to stressing thereof; and

removing the sacrificial metal layer from the wafer prior to performing the wafer probe procedure.

16.-26. (Cancelled)